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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/714,285	11/17/2000	Miyoshi Saito	100021-00033	6273

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EXAMINER	
TSE, YOUNG TOI	
ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/714,285	SAITO ET AL.	
	Examiner	Art Unit	
	YOUNG T. TSE	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 29 April 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 17-80 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 40,42-47 and 56-64 is/are allowed.
- 6) Claim(s) 17-39,48-55 and 65-80 is/are rejected.
- 7) Claim(s) 41 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 17 November 2000 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. 09/062,586.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed April 29, 2005 have been fully considered but they are not persuasive.

The Applicants argue Figures 6A-6B, 7B, 8-12 and 15-17 as "Related Art" rather than "Prior Art". Therefore, the Applicants are requested to label Figures 6A-6B, 7B, 8-12 and 15-17 as "Related Art".

With respect to the 112, first paragraph, the Applicants argue that claims 17 and 65 correspond to Fig. 68 or the 12th embodiment of the disclosure and claim 20 relates to Figs. 13 to 20 or the first and second embodiments of the present disclosure.

Claims 17 and 65 are directly related to apparatus claims, however, Figure 68 shows waveforms only which can not read on any of the claimed subject matter of the independent claims 17 and 65 and also the dependent claims 18-19 and 66-80.

Claim 20 is also an apparatus claim which seems not read on all the Figures 13-20, the Applicants are requested to point out exactly which claimed elements correspond to which block elements of the figures, claims 21-33 depend upon claim 20.

However, the rejection of claims 40-64 under 112, first paragraph has been withdrawn.

With respect to the 35 U.S.C. 102 art rejection of claims 17-19, 65 and 69, the Applicants argue that claim 17 recites a signal transmission system comprising, among other features, wherein, when writing, at least during a portion of a period when a select

signal for connecting said data bus to said sense amplifier is being supplied a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier. Claim 65 recites a semiconductor memory device comprising, among other features, when writing, at least during a portion of a period when a select signal for connecting said data bus to said sense amplifier is being supplied, a bit line connected to said sense amplifier for amplification is disconnected from said sense amplifier, thereby allowing information on said data bus to be transferred at high speed into said sense amplifier. Therefore, the prior art fails to disclose or suggest at least the above-mentioned features of the invention.

Akiyama discloses a diagram of a memory block structure in Figure 2 and a memory structure in Figure 3. Referring to Figure 3, the memory structure comprises a memory unit 210, a data selector 300 and an input/output selector 310. The memory unit 210 comprises at least memory cells 220, selected word lines 221, and bit lines 222 for storing data or bit structures with the data selector 300 and the input/output selector 310. The data selector 300 comprises a sense amplifier circuit and a write amplifier circuit. For reading of data, a data signal of the memory cell 210 connected to the selected word line 221 appears on the bit line 222, and is fed to the sense amplifier circuit through a reading column select switch 240, then is transmitted to the next step sense circuit. On the other hand, for writing of data, an output signal of the write amplifier circuit is fed to the bit line 222 through a writing column select switch 230, and is written to the memory cell 220. The output signal of the input/output selector 310

controls the operations of the write amplifier circuit and the sense amplifier circuit. See column 3, line 56 to column 4, line 13.

With respect to the 35 U.S.C. 102 art rejection of claim 48, the Applicants argue that claim 48 recites a semiconductor memory device comprising, among other features, a state latch circuit for holding at least two states consisting of a CURRENT state indicating a bus currently in an active state and a NEXT state indicating a bus to be selected and activated next, or four states consisting of said CURRENT state, said NEXT state, a STANDBY state indicating a bus in a standby state, and a PREVIOUS state indicating a bus just deactivated. Kurtze merely discloses an interface enabling asynchronous data processing elements to be interconnected using an interconnection protocol, and wherein control information is double buffered and has two states, an "active" state and a "shadow" state. As clearly described on column 9, lines 56 through 59 of Kurtze, the active state contains the current state used in processing, while the shadow state is the control information for the next function to be performed. It is submitted that the "active" and "shadow" states of Kurtze constitute a queue of operations to be performed in the processing elements, and therefore, when the current "active" operation is completed, the queue proceeds one stage and the information stored in the "shadow" register becomes active. Therefore, the contents of the "active" and "shadow" registers of Kurtze may be consistent or different, and when the contents of the "active" and "shadow" registers are the same, the same operation is continuously performed in Kurtze.

Kurtze clearly discloses a processing element 200 in Figure 3A and teaches the processing element 200 receives control information from control registers 243. The control registers are loaded via a bus connected to the host computer as indicated as 245. The structures of the control registers 243 are shown in Figures 4A and 4B. The control information has two states, an “active” state and a “shadow” state. The active state contains the state used in processing, while the shadow state is the control information for the next function to be performed. See column 9, lines 24-59. Although Kurtze does not explicitly use the term the current state indicating a bus currently in an active state and the shadow state indicating the bus to be selected and activated next. Inherently, the current state used in processing means currently in an active state, while the shadow state is the control information for the next function to be performed means the next state indicating the bus to be selected and activated next.

Drawings

2. Figures 6A-6B, 7B, 8-12, and 15-17 should be designated by a legend such as -- Related Art-- because only that which is old is illustrated (see the Brief Description of the Drawings). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 22, 26, 33, 39, 41, 48, 56, and 80 are objected to because of the following informalities:

In claim 22, line 4, "said transmission line" should be "said signal transmission line".

In claim 26, line 6, "performs" should be "said first partial response amplifier performs".

In claim 33, lines 5 and 6, "a bus" should be "the bus".

In claim 39, line 2, "a continuous" should be "continuous".

In claim 41, lines 4, 6, and 6-7, "a bus" should be "the bus".

In claim 48, lines 4, 6, and 7, "a bus" should be "the bus".

In claim 56, line 3, "bus" should be "bus,".

In claim 80, line 2, "a plurality" should be "plurality".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 17-39 and 65-80 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicants are requested to clarify the difference between the present invention and the prior art as shown in Figures 1-11 and 15-18 in the specification in order to enable a person skill in the art to understand the present invention as recited in claims 17-39 and 65-80.

Applicants are also requested to clarify that which claim(s) corresponds to which embodiment(s) of the present invention since the instant application includes a total of 18 different embodiments or inventions. See the Brief Description of the Drawings.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 24-26, 29-30, 34, 48-55, and 74 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 24 (line 4), claim 34 (line 3), claim 51 (line 4), and claim 74 (line 2), the phrases "the intersymbol interference component elimination", "said data bus", "said off state", and "the data bus precharge" all lack antecedent basis.

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In claim 29, lines 3, 4 and 9, Applicants are requested to clarify the difference of "a driver" recited in three different areas. Further, the last sentence of claim 29 is not understood.

In claim 48, the state latch circuit lacks connection or cooperation of the plurality of blocks.

Claims 25-26, 30, 49-50 and 52-55 depend upon claims 24, 29 and 48.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 17-19, 65 and 69 are rejected under 35 U.S.C. 102(e) as being anticipated by Akiyama et al..

Akiyama et al. (U.S. Patent No. 5,638,335) discloses a memory device in Figure 3 comprising a memory array having a plurality of bits and a plurality of memory blocks.

With respect to claims 17-19, 65 and 69, the memory device comprises a data selector has at least a column select switch for connecting or disconnecting bit lines connected to memory cells with or from a write amplifier and a sense amplifier. See Figure 3 and claim 5.

10. Claim 48 is rejected under 35 U.S.C. 102(e) as being anticipated by Kurtze et al..

Kurtze et al. (U.S. Patent No. 6,105,083) discloses a processing element 200 in Figure 3A receives a control information from control registers 243 which are loaded via a bus connected to a host computer as indicated at 245.

With respect to claim 48, the control registers 243 may be implemented using the register constructions shown in Figures 4A and 4B. The control information may be double buffered and thus have two states, an "active" state and a "shadow" state. The active state contains the current state used in processing, while the shadow state is the control information for the next function to be performed. See column 9, lines 50-59.

Allowable Subject Matter

11. Claims 40, 42-47 and 56-64 are allowed.

12. Claim 41 would be allowable if rewritten or amended to overcome the objection(s) set forth in this Office action.

13. Claims 49-55 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

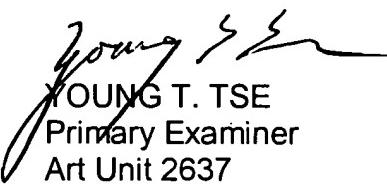
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday-Thursday and alternative Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The Central FAX Number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



YOUNG T. TSE
Primary Examiner
Art Unit 2637